Rev 2; 4/08

DALLAS SEMICONDUCTOR MAXIM

Accurate I²C RTC with Integrated TCXO/Crystal/FRAM

General Description

The DS32B35/DS32C35 accurate real-time clocks (RTC) are clock/calendars that include an integrated temperature-compensated crystal oscillator (TCXO), crystal, and a bank of nonvolatile memory (FRAM) in a single package. The nonvolatile memory is available in two densities: 2048 x 8 and 8192 x 8 bits. The integration of the crystal resonator enhances the long-term accuracy of the devices as well as reduces the piece part count in a manufacturing line. The devices operate as a slave device on an I²C serial interface, and are available in both commercial and industrial temperature ranges in a 300-mil, 20-pin SO package.

The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year.

The DS32B35/DS32C35 include a bank of nonvolatile memory that does not require a backup energy source to maintain memory contents. In addition, there are no read or write cycle limitations. The memory array can be accessed at maximum cycle rates for the life of the product with no wear-out mechanisms.

Other device features include two time-of-day alarms, a selectable output that provides either an interrupt or programmable square wave, and a calibrated 32.768kHz square-wave output. A reset input/output pin provides a power-on reset for other devices. Additionally, the reset pin is monitored as a pushbutton input for generating a reset externally.

A precision temperature-compensated voltage reference and comparator circuit monitor the status of V_{CC} to detect power failures, to provide a reset output, and to automatically switch to the backup supply for the RTC/TCXO when necessary. Additionally, the $\overline{RST}$ pin is monitored as a pushbutton input for generating a reset externally.

Applications

Servers	Utility Power Meters
Telematics	GPS

Typical Operating Circuit, Pin Configuration, and Selector Guide appear at end of data sheet.

Features

- **Integrated 32.768kHz Crystal**
- **Fast (400kHz) I²C Interface**
- **RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Valid Up to 2100**
- **RTC Accuracy ±2ppm from 0°C to +40°C**
- **RTC Accuracy ±3.5ppm from -40°C to 0°C and +40°C to +85°C**
- **Nonvolatile Memory with 10 Years of Guaranteed Backup Time and Write Protection**
- **Two Available Densities of Nonvolatile Memory**
  2048 Bytes (DS32B35)
  8192 Bytes (DS32C35)
- **No Cycle Limitations on Memory**
- **Power-Switching Circuit Selects Between Main Power and Battery Backup for the RTC**
- **Programmable Square Wave with Frequency of 32.768kHz, 8.192kHz, 4.096kHz, or 1Hz**
- **Two Time-of-Day Alarms**
- **Reset Output/Pushbutton Reset (Debounced) Input**
- **Programmable Output Provides Interrupt or Square Wave**
- **Calibrated 32.768kHz Open-Drain Output**
- **Temp Sensor with ±3°C Accuracy**
- **3.3V Operating Voltage**
- **Commercial and Industrial Temperature Ranges**
- **300-mil, 20-Pin SO Package**
- **Underwriters Laboratories (UL) Recognized**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS32B35-33#	0°C to +70°C	20 SO
DS32B35-33IND#	-40°C to +85°C	20 SO
DS32C35-33#	0°C to +70°C	20 SO
DS32C35-33IND#	-40°C to +85°C	20 SO

 # Denotes a RoHS-compliant device that may include lead that is exempt under RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes. A "#" anywhere on the top mark denotes a RoHS-compliant device.

Accurate I²C RTC with Integrated TCXO/Crystal/FRAM

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.3V to +5.0V
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+125°C
Storage Temperature Range.....-40°C to +85°C
Lead Temperature (soldering, 10s).....+260°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.70	3.3	3.63	V
Battery Voltage	V_{BAT}	(Note 3)	2.3	3.0	3.6	V
Input High Voltage	V_{IH}	(Note 4)	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		+0.3 x V_{CC}	V

ELECTRICAL CHARACTERISTICS

(**V_{CC} = 2.7V to 3.63V**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Supply Current	I_{CCA}	V_{CC} = 3.63V, SCL = 400kHz (Note 5)	Accessing RTC			260	µA
			Accessing FRAM memory			260	
Standby Supply Current	I_{CCS}	V_{CC} = 3.63V, SCL = 0kHz, 32kHz on, SQW off (Note 5)				110	µA
Temperature Conversion Current	I_{TC}	V_{CC} = 3.65V, SCL = 0kHz, 32kHz on, SQW off				575	µA
Power-Fail Voltage	V_{PF}			2.45	2.575	2.70	V
Logic 0 Output 32kHz, $\overline{INT}$/SQW, SDA	V_{OL}	I_{OL} = 3mA				0.4	V
Logic 0 Output $\overline{RST}$	V_{OL}	I_{OL} = 1mA				0.4	V
Output Leakage Current 32kHz, $\overline{INT}$/SQW, SDA	I_{LEAK}	Output high impedance		-1		+1	µA
Input Leakage SCL	I_{LI}			-1		+1	µA
$\overline{RST}$ I/O Leakage	I_{OL}	$\overline{RST}$ high impedance (Note 6)		-200		+10	µA
WP Input Resistance	R_{IN}	V_{IN} = $V_{IL(MAX)}$		50			kΩ
		V_{IN} = $V_{IH(MIN)}$		1			MΩ

ELECTRICAL CHARACTERISTICS (continued)

(**V_{CC} = 2.7V to 3.63V**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BAT} Leakage Current (V_{CC} Active)	I_{BATLKG}				25	100	nA
Output Frequency	f_{OUT}	V_{CC} = 3.3V or V_{BAT} = 3.3V			32.768		kHz
Frequency Stability vs. Temperature	$\Delta f/f_{OUT}$	V_{CC} = 3.3V or V_{BAT} = 3.3V	-40°C to 0°C	-3.5		+3.5	ppm
			0°C to +40°C	-2		+2	
			-40°C to +85°C	-3.5		+3.5	
Frequency Stability vs. Voltage	$\Delta f/V$				1		ppm/V
Frequency Sensitivity per LSB	$\Delta f/LSB$	Specified at:	-40°C		0.7		ppm
			+25°C		0.1		
			+70°C		0.4		
			+85°C		0.8		
Temperature Sensor Accuracy	Temp	V_{CC} = 3.3V or V_{BAT} = 3.3V		-3		+3	°C
Temperature Conversion Time	t_{CONV}				125	200	ms

ELECTRICAL CHARACTERISTICS

(**V_{CC} = 0V, V_{BAT} = 2.3V to 3.6V**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Battery Current	I_{BATA}	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = 400kHz (Note 5)	V_{BAT} = 3.6V			70	µA
Timekeeping Battery Current	I_{BATT}	$\overline{EOSC}$ = 0, BBSQW = 0, EN32kHz = 1, SCL = SDA = 0V or SCL = SDA = V_{BAT} (Note 5)	V_{BAT} = 3.6V		0.84	3.0	µA
Temperature Conversion Current	I_{BATTC}	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = SDA = 0V or SCL = SDA = V_{BAT}	V_{BAT} = 3.6V			575	µA
Data-Retention Current (RTC/TCXO Registers)	I_{BATDR}	$\overline{EOSC}$ = 1, SCL = SDA = 0V, +25°C				100	nA

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.63V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Conditions	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 7)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Low Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Data Hold Time (Notes 8, 9)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 10)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Setup Time for Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals (Note 11)	t_R	Fast mode	20 + 0.1C_B		300	ns
		Standard mode			1000	
Fall Time of Both SDA and SCL Signals (Note 11)	t_F	Fast mode	20 + 0.1C_B		300	ns
		Standard mode			300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line (Note 11)	C_B				400	pF
I/O Capacitance $\overline{INT}$/SQW, 32kHz, SCL, SDA	$C_{I/O}$	Outputs = high impedance		10		pF
				18		
Pushbutton Debounce	PB_{DB}	(See the *Pushbutton Reset Timing* diagram)		250		ms
Reset Active Time	t_{RST}			250		ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 12)		100		ms
FRAM Data Retention	t_{DR}		10			Years

POWER-SWITCH CHARACTERISTICS

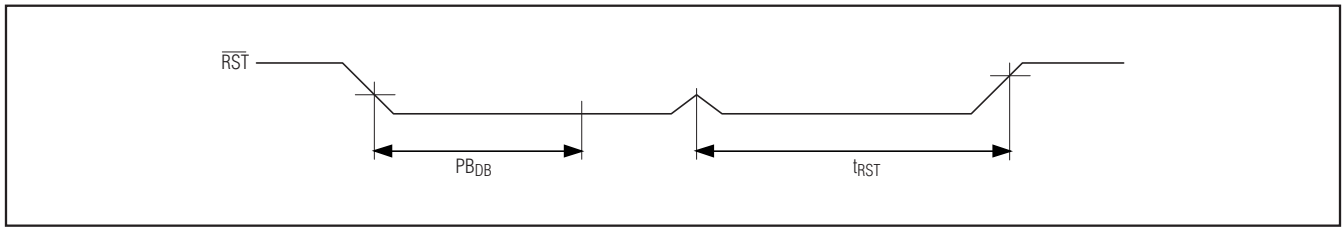
(T_A = -40°C to +85°C, Note 1, see the *Power-Switch Timing* diagram.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs
Recovery at Power-Up	t_{REC}	(Note 13)			300	ms

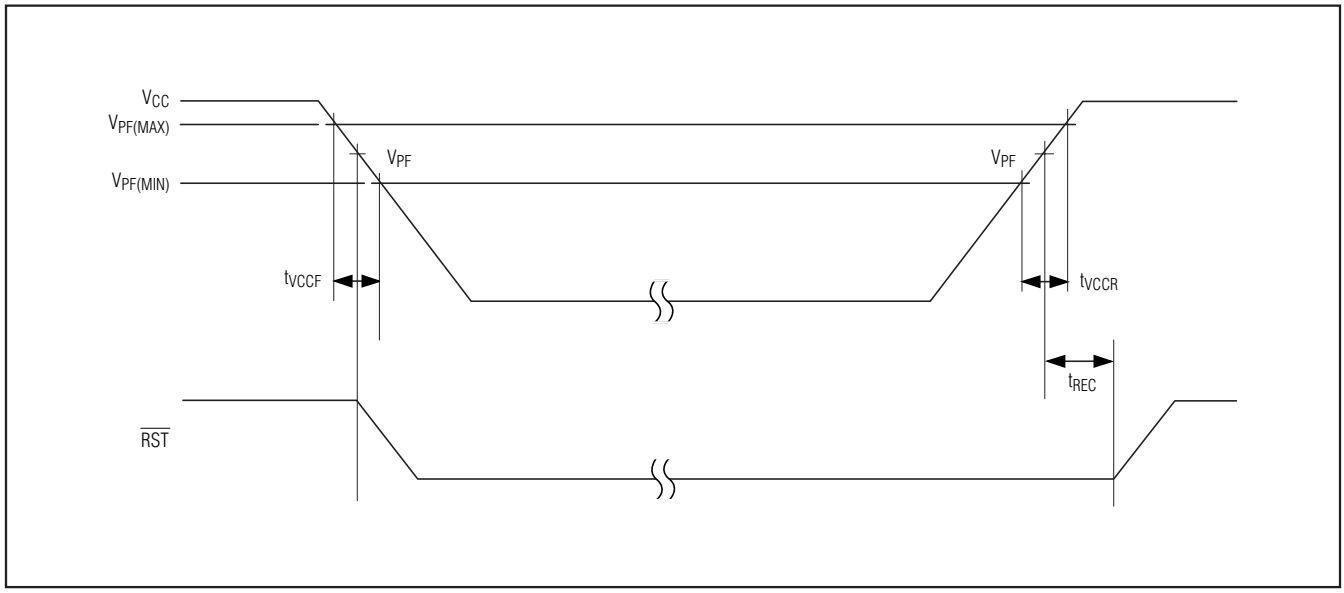
WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: To minimize current drain on V_{BAT} when the internal supply is switched to V_{BAT}, the V_{IH} minimum must be higher than V_{BAT} - 0.6V. Otherwise, there is significant current drain due to the input stage at the SCL and SDA pins.
Note 4: The pullup resistor voltage on the 32kHz and $\overline{INT}$/SQW pins can be up to 5.5V maximum regardless of the voltage on V_{CC}.
Note 5: Current is the averaged input current, which includes the temperature conversion current.
Note 6: The $\overline{RST}$ pin has an internal 50kΩ (nominal) pullup resistor to V_{CC}.
Note 7: After this period, the first clock pulse is generated.
Note 8: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to as the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 9: The maximum $t_{HD:DAT}$ needs only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 10: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
Note 11: C_B—total capacitance of one bus line in pF.
Note 12: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leq V_{CC} \leq V_{CC(MAX)}$ and $2.0V \leq V_{BAT} \leq 3.6V$.
Note 13: This delay applies only if the oscillator is enabled and running. If the $\overline{EOSC}$ bit is a 1, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. The state of $\overline{RST}$ does not affect the I²C interface, RTC, TCXO, or FRAM operation.

Pushbutton Reset Timing



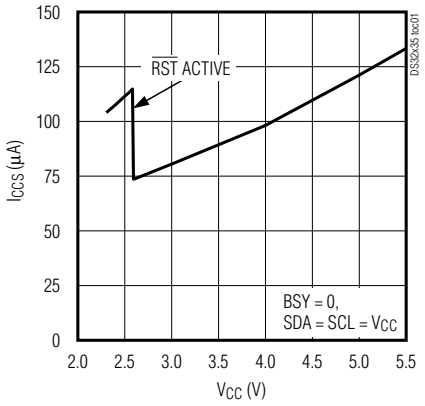
Power-Switch Timing



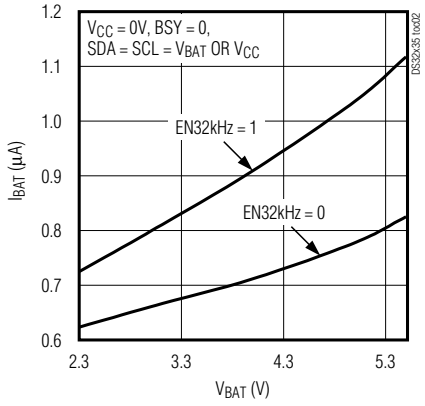
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

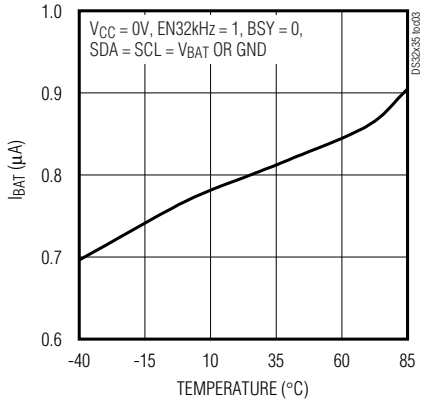
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



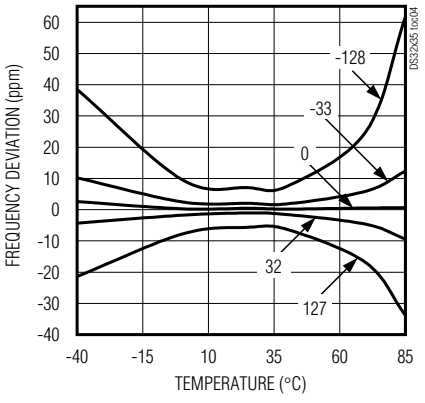
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

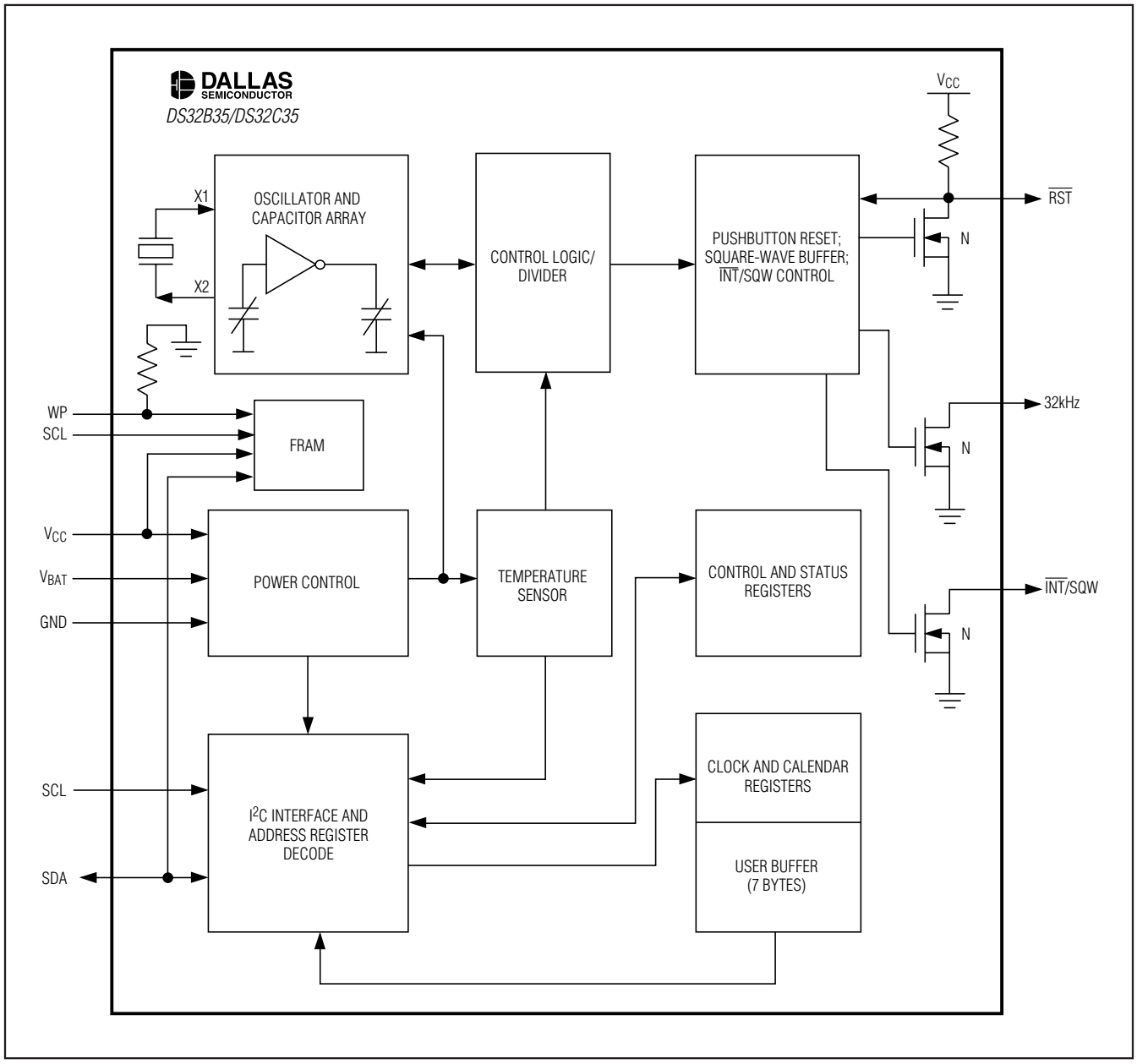


FREQUENCY DEVIATION vs. TEMPERATURE vs. AGING VALUE



Accurate I²C RTC with Integrated TCXO/Crystal/FRAM

Block Diagram



Pin Description

PIN	NAME	FUNCTION
1	WP	Write Protect. When WP is high, the entire FRAM memory array is write protected. When WP is low, all addresses can be written. This pin is internally pulled down.
2, 7–14	N.C.	No Connection. Must be connected to ground.
3	32kHz	32kHz Output. This open-drain pin requires an external pullup resistor. When enabled, the output operates on either power supply. It can be left open if not used.
4	V_{CC}	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1µF to 1.0µF capacitor.
5	$\overline{INT}$/SQW	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor connected to V_{CC} or another supply of 5.5V or less. It can be left open if not used. This multifunction pin is determined by the state of the INTCN bit in the Control register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by the RS2 and RS1 bits. When INTCN is set to logic 1, a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW pin (if the alarm is enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled.
6	$\overline{RST}$	Active-Low Reset. This pin is an open-drain input/output. It indicates the status of V_{CC} relative to the V_{PF} specification. As V_{CC} falls below V_{PF}, the $\overline{RST}$ pin is driven low. When V_{CC} exceeds V_{PF}, for t_{RST}, the open-drain pulldown transistor is shut off, and the internal pullup resistor pulls the $\overline{RST}$ pin to V_{CC}. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50kΩ nominal value pullup resistor to V_{CC}. No external pullup resistors should be connected. If the $\overline{EOSC}$ bit is 1, t_{REC} is bypassed and $\overline{RST}$ immediately goes high.
15, 19	GND	Ground. Must be connected together to ground.
16	V_{BAT}	Backup Power-Supply Input. This pin should be decoupled using a 0.1µF to 1.0µF low-leakage capacitor. If the I²C interface is inactive whenever the device is powered by the V_{BAT} input, the decoupling capacitor is not required. If V_{BAT} is not used, connect to ground. UL recognized to ensure against reverse charging when used with a lithium battery. Go to www.maxim-ic.com/qa/info/ul.
17	SDA	Serial Data Input/Output. This pin is the data input/output for the I²C serial interface. This open-drain pin requires an external pullup resistor.
18, 20	SCL	Serial Clock Input. These pins are the clock input for the I²C serial interface and are used to synchronize data movement on the serial interface.

Detailed Description

The DS32B35/DS32C35 accurate RTCs are clock/calendars that include an integrated TCXO, crystal, and a bank of nonvolatile memory (FRAM) in a single package. The nonvolatile memory is available in two sizes: 2048 x 8 or 8192 x 8 bits. The integration of the crystal resonator enhances the long-term accuracy of the device as well as reduces the piece part count in a manufacturing line. The devices are available in both commercial and industrial temperature ranges and is offered in a 300-mil, 20-pin SO package.

The DS32B35/DS32C35 include a bank of nonvolatile memory that do not require a backup energy source to maintain the memory contents. In addition, there are no read or write cycle limitations. The memory array can be accessed at maximum cycle rates for the life of the product with no wear-out mechanisms.

A precision temperature-compensated reference and comparator circuit monitors the status of V_{CC} and automatically switches to the backup supply when necessary. Other device features include two time-of-day alarms, a selectable output that provides either an interrupt or programmable square wave, and a calibrated 32.768kHz square-wave output. A reset input/output pin provides a power-on reset. Additionally, the reset pin is monitored as a pushbutton input for generating a reset externally. The devices are accessed through an I²C serial interface.

Accurate I²C RTC with Integrated TCXO/Crystal/FRAM

Operation

The *Block Diagram* shows the main elements of the DS32B35/DS32C35. The nine blocks can be grouped into six functional groups: TCXO, power control, pushbutton function, RTC, I²C interface, and FRAM. Their operations are described separately in the following sections.

32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction in the AGE register, and then sets the capacitance selection registers. New values, including changes to the AGE register, are loaded only when a change in the temperature value occurs, or when a user-initiated temperature conversion is completed. The temperature is read on initial application of V_{CC} and once every 64 seconds afterwards while the device is powered by either V_{CC} or V_{BAT}.

Power Control

This function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. When V_{CC} is greater than V_{PF}, the part is powered by V_{CC}. When V_{CC} is less than V_{PF} but greater than V_{BAT}, the RTC is powered by V_{CC}. If V_{CC} is less than V_{PF} and is less than V_{BAT}, the device is powered by V_{BAT}. See Table 1.

The RTC can be accessed when the device is powered by either V_{CC} or V_{BAT}. The FRAM is only accessible when the device is powered by V_{CC}. The FRAM must not be accessed when $V_{CC} < V_{CC(MIN)}$.

Table 1. Device Operation

SUPPLY CONDITION	POWERED BY	FRAM ACCESS*	RTC ACCESS
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	V_{BAT}	No	Yes
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}	No	Yes
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	V_{CC}	Yes	Yes
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}	Yes	Yes

**Read/write access is not inhibited by the device, but must not be done to avoid FRAM data errors.*

To preserve the battery, the first time V_{BAT} is applied to the device, the oscillator will not start up until V_{CC} exceeds V_{PF}, or until a valid I²C address is written to the part. Typical oscillator startup time is less than one second. Approximately 2 seconds after V_{CC} is applied, or a valid I²C address is written, the device makes a temperature measurement and applies the calculated correction to the oscillator. Once the oscillator is running, it continues to run as long as a valid power source is available (V_{CC} or V_{BAT}), and the device continues to measure the temperature and correct the oscillator frequency every 64 seconds.

On the first application of power (V_{CC}) or when a valid I²C address is written to the part (V_{BAT}), the time and date registers are reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS).

Pushbutton Reset Function

The device provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the device is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge transition is detected, the device debounces the switch by pulling $\overline{RST}$ low. After the internal timer has expired (PB_{DB}), the device continues to monitor the $\overline{RST}$ line. If the line is still low, the device continuously monitors the line looking for a rising edge. Upon detecting release, the device forces the $\overline{RST}$ pin low and holds it low for t_{RST}.

$\overline{RST}$ is also used to indicate a power-fail condition. When V_{CC} is lower than V_{PF}, an internal power-fail signal is generated, which forces the $\overline{RST}$ pin low. When V_{CC} returns to a level above V_{PF}, the $\overline{RST}$ pin is held low for t_{REC} to allow the power supply to stabilize. If the oscillator is not running (see the *Power Control* section) when V_{CC} is applied, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. The state of $\overline{RST}$ does not affect the operation of the TCXO, I²C interface, FRAM, or RTC functions.

Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an $\overline{AM}$/PM indicator.

The clock provides two programmable time-of-day alarms and a programmable square-wave output. The $\overline{INT}$/SQW pin either generates an interrupt due to alarm condition or outputs a square-wave signal and the selection is controlled by the bit INTCN.

I²C Interface

The FRAM I²C interface is accessible whenever V_{CC} is at a valid level. The RTC I²C interface is accessible whenever either V_{CC} or V_{BAT} is at a valid level. If a microcontroller connected to the device resets because of a loss of V_{CC} or other event, it is possible that the microcontroller and the RTC I²C communications could become unsynchronized, e.g., the microcontroller resets while reading data from the RTC. When the microcon-

troller resets, the RTC I²C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

FRAM

The serial FRAM memory is logically organized as a 2048 x 8 or 8192 x 8 memory array and is accessed using the I²C interface. Functional operation of the FRAM is similar to serial EEPROMs with the major difference being its superior performance on writes. The memory is read or written at the speed of the I²C interface. It is not necessary to poll the device for a ready condition during writes.

Due to the different memory densities, the I²C addressing technique is different for each version of the device. See the *I²C Serial Data Bus* section for details.

Table 2. Memory Slave Address

DEVICE	SLAVE ADDRESS
DS32B35	1010 $A_{10}A_9A_8$R
DS32C35	1010 000R

R = Read/write select bit

Warning: The FRAM does not inhibit reads or writes when V_{CC} is below the minimum operating voltage. FRAM reads are destructive, that is, when a read is performed, the device internally writes the memory back to the original value. The FRAM must not be read or written when V_{CC} is below the minimum operating voltage; otherwise, the memory cells may not be fully programmed, and the data may not be retained.

RTC Address Map

Table 3 shows the RTC address map for the timekeeping registers. During a multibyte access, when the address pointer reaches the end of the register space, it wraps around to location 00h. On an I²C START or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Table 3 illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The device can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic-high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START and when the register pointer rolls over to zero. The time information is read from these secondary registers while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the device. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided that the oscillator is already running.

Accurate I²C RTC with Integrated TCXO/Crystal/FRAM

Table 3. RTC Register Map

ADDRESS	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Hours	1–12 + $\overline{AM}$/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	01–31
05h	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06h	10 Year				Year				Year	00–99
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Alarm 1 Hours	1–12 + $\overline{AM}$/PM 00–23
0Ah	A1M4	DY/$\overline{DT}$	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	1–31
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Alarm 2 Hours	1–12 + $\overline{AM}$/PM 00–23
0Dh	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	1–31
0Eh	$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0Fh	OSF	0	0	0	EN32kHz	BSY	A2F	A1F	Control/Status	—
10h	Sign	Data	Data	Data	Data	Data	Data	Data	Aging Offset	—
11h	Sign	Data	Data	Data	Data	Data	Data	Data	MSB of Temp	—
12h	Data	Data	0	0	0	0	0	0	LSB of Temp	—

Note: *Unless otherwise specified, the registers' state is not defined when power is first applied. Bits indicated as 0 can be written to a 1 or 0, but always read back as 0.*

Alarms

The DS32B35/DS32C35 contain two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the Control register) to activate the $\overline{INT}$/SQW output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 4). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 4 shows the possible settings. Configurations not listed in the table will result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag ("A1F") or ("A2F") bit is set to logic 1. If the corresponding alarm interrupt enable ("A1IE") or ("A2IE") is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition will activate the $\overline{INT}$/SQW signal.

Table 4. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second.
X	1	1	1	0	Alarm when seconds match.
X	1	1	0	0	Alarm when minutes and seconds match.
X	1	0	0	0	Alarm when hours, minutes, and seconds match.
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match.
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match.

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute).
X	1	1	0	Alarm when minutes match.
X	1	0	0	Alarm when hours and minutes match.
0	0	0	0	Alarm when date, hours, and minutes match.
1	0	0	0	Alarm when day, hours, and minutes match.

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Control Register (0Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE

Special-Purpose Registers

Control Register (0Eh)

Bit 7: Enable Oscillator ($\overline{EOSC}$). When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the device switches to V_{BAT}. This bit is clear (logic 0) when power is first applied. When the device is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{EOSC}$ bit.

Bit 6: Battery-Backed Square-Wave Enable (BBSQW). When set to logic 1 and the device is being powered by the V_{BAT} pin, this bit enables the square-wave or interrupt output when V_{CC} is absent. When BBSQW is logic 0, the $\overline{INT}$/SQW pin goes high impedance when V_{CC} falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

Bit 5: Convert Temperature (CONV). When the device is in idle state, setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance load for the oscillator. This can only happen when a conversion is not already in progress. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second update cycle.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. Table 5 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (8.192kHz) when power is first applied.

Bit 2: Interrupt Control (INTCN). This bit controls the $\overline{INT}$/SQW signal. When the INTCN bit is set to logic 0, a square wave is output on the $\overline{INT}$/SQW pin. When the INTCN bit is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW output (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to logic 1 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{INT}$/SQW (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the $\overline{INT}$/SQW signal. The A1IE bit is disabled (logic 0) when power is first applied.

Table 5. Interrupt/Square-Wave Output

INTCN	RS2	RS1	$\overline{INT}$/SQW OUTPUT	INTCN	A2IE	A1IE
0	0	0	1Hz	0	X	X
0	0	1	1.024kHz	0	X	X
0	1	0	4.096kHz	0	X	X
0	1	1	8.192kHz	0	X	X
1	X	X	A1F	1	0	1
1	X	X	A2F	1	1	0
1	X	X	A2F + A1F	1	1	1

Status Register (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	0	0	0	EN32kHz	BSY	A2F	A1F

Status Register (0Fh)

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltages present on both V_{CC} and V_{BAT} are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off in battery-backed mode.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 3: Enable 32kHz Output (EN32kHz). This bit controls the status of the 32kHz pin. When set to logic 1, the 32kHz pin is enabled and outputs a 32.768kHz square-wave signal. When set to logic 0, the 32kHz pin goes to a high-impedance state. The initial power-up state of this bit is logic 1, and a 32.768kHz square-wave signal appears at the 32kHz pin after a V_{CC} is applied to the device.

Bit 2: Busy (BSY). This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the device is in the 1-minute idle state. When active, the BSY signal prevents the CONV signal from aborting the execution of the TCXO algorithm and starting a new execution of TCXO function.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is logic 1 and the INTCN bit is set to logic 1, the $\overline{INT}$/SQW pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is logic 1 and the INTCN bit is set to logic 1, the $\overline{INT}$/SQW pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Aging Offset Register (10h)

The Aging Offset register provides an 8-bit code to add to the codes in the capacitance array registers. The code is encoded in two's complement. One LSB represents one small capacitor to be switched in or out of the capacitance array at the crystal pins.

The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is distorted by the values used in this register. At +23°C, one LSB typically provides approximately 0.1ppm change in frequency.

Aging Offset (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sign	Data	Data	Data	Data	Data	Data	Data

Temperature Register (Upper Byte) (11h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sign	Data	Data	Data	Data	Data	Data	Data

Temperature Register (Lower Byte) (12h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Data	Data	0	0	0	0	0	0

Temperature Registers (11h–12h)

Temperature is represented as a 10-bit code with a resolution of +0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two's complement format. The upper 8 bits are at location 11h, and the lower 2 bits are in the upper nibble at location 12h. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion. New temperature readings are stored in this register.

FRAM Address Map

During a multibyte access, the address pointer wraps around to location 00h when it reaches the end of the register space.

DS32B35 FRAM Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RANGE
000h	D7	D6	D5	D4	D3	D2	D1	D0	00–FF
:	:	:	:	:	:	:	:	:	:
7FFh	D7	D6	D5	D4	D3	D2	D1	D0	00–FF

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied.*

DS32C35 FRAM Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RANGE
000h	D7	D6	D5	D4	D3	D2	D1	D0	00–FF
:	:	:	:	:	:	:	:	:	:
1FFFh	D7	D6	D5	D4	D3	D2	D1	D0	00–FF

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied.*

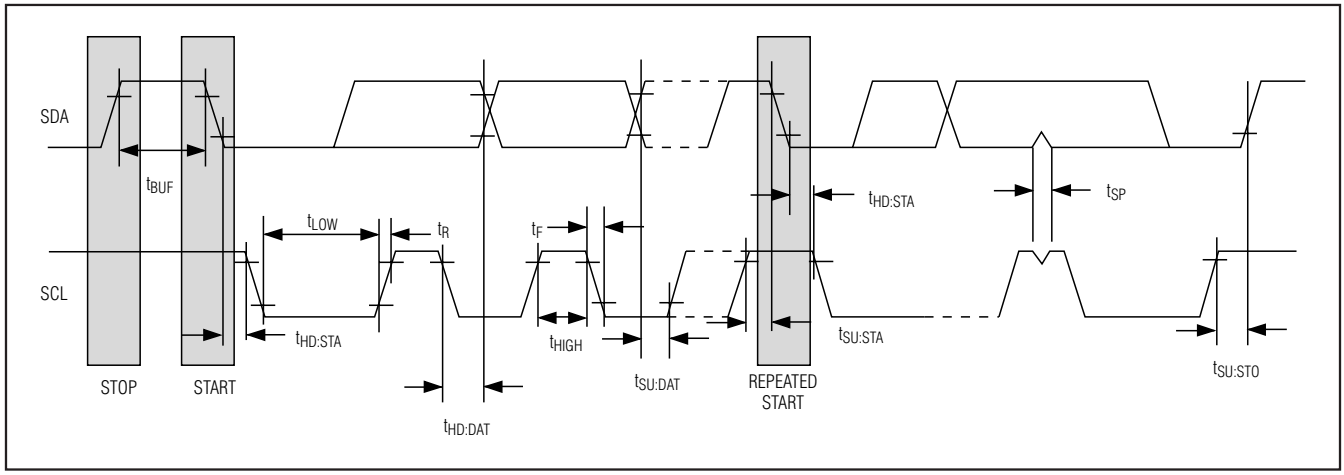

Figure 1. Data Transfer on I²C Serial Bus

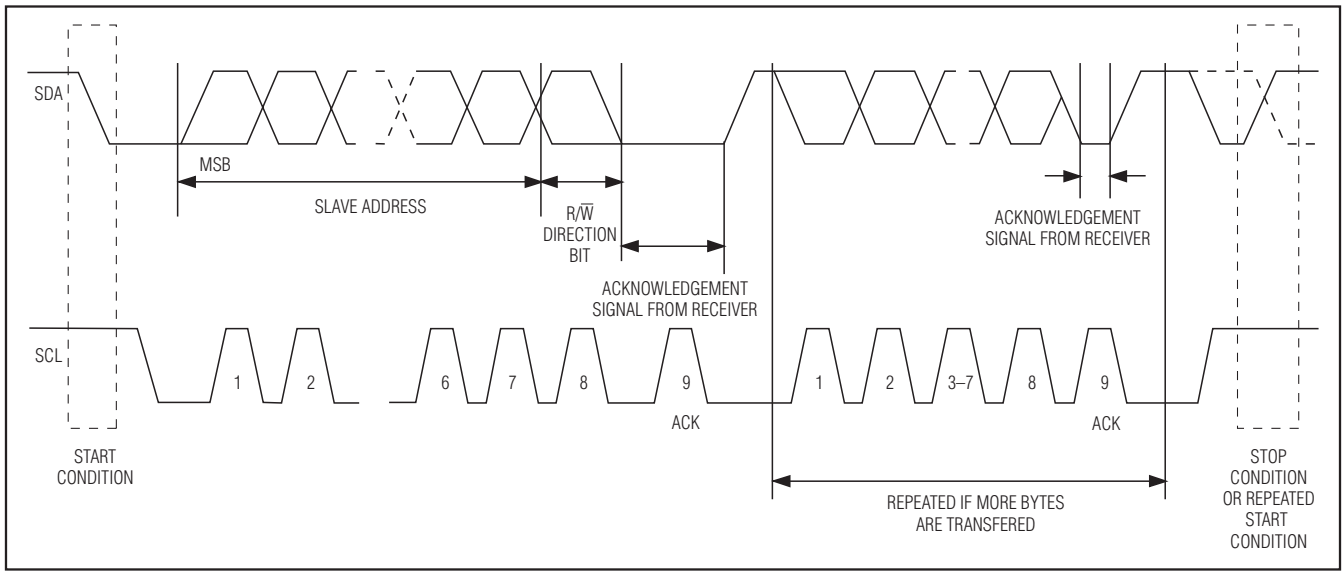

Figure 2. I²C Data Transfer Overview

I²C Serial Data Bus

The DS32B35/DS32C35 support a bidirectional I²C bus and data transmission protocol (Figure 1). A device that sends data onto the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The device operates as a slave on the I²C bus. Connections to the bus are made through the SCL input and open-drain SDA I/O lines. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS32B35/DS32C35 work in both modes.

The following bus protocol has been defined (Figure 2):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

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Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

   The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The DS32B35/DS32C35 can operate in the following two modes:

1) **Slave receiver mode (DS32B35/DS32C35 write mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figures 3, 5, and 7). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains one of the 7-bit device addresses. The slave address is 1101000 for the RTC. For the DS32B35 FRAM, the first four bits are 1010, and the next three bits select one of eight blocks of data (see Table 2). For the DS32C35 FRAM, the first seven bits are 1010000. Each slave address is followed by the direction bit (R/$\overline{W}$), which is zero for a write. After receiving and decoding the slave address byte, the device outputs an acknowledge on the SDA line. After the device acknowledges the slave address and write bit, the master transmits a register address to the device. For the DS32C35, the master transmits two bytes for the register address information. This sets the register pointer on the device. After setting the register address, the master then transmits zero or more bytes of data with the device acknowledging each byte received. The master generates a STOP condition to terminate the data write.

2) Slave transmitter mode (DS32B35/DS32C35 read mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. The device transmits serial data on SDA while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (see Figure 4). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains one of the 7-bit device addresses. The slave address is 1101000 for the RTC. For the DS32B35 FRAM, the first four bits are 1010, and the next three bits select one of eight blocks of data (see Table 2). Each slave address is followed by the direction bit (R/$\overline{W}$), which is one for a read. After receiving and decoding the slave address byte, the device outputs an acknowledge on the SDA line. The device then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The device must receive a "not acknowledge" to end a read. The register pointer can be set prior to a data read by initiating a slave receiver mode sequence, with no data bytes transmitted after the register address data.

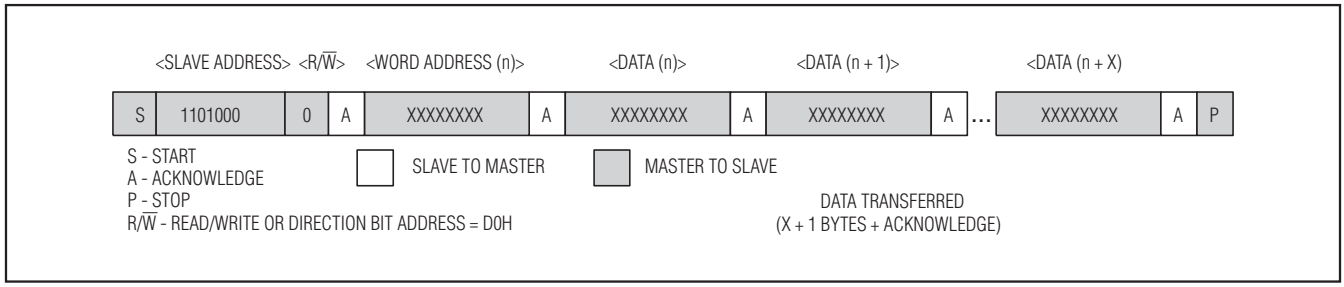

Figure 3. Data Write—RTC Slave Receiver Mode

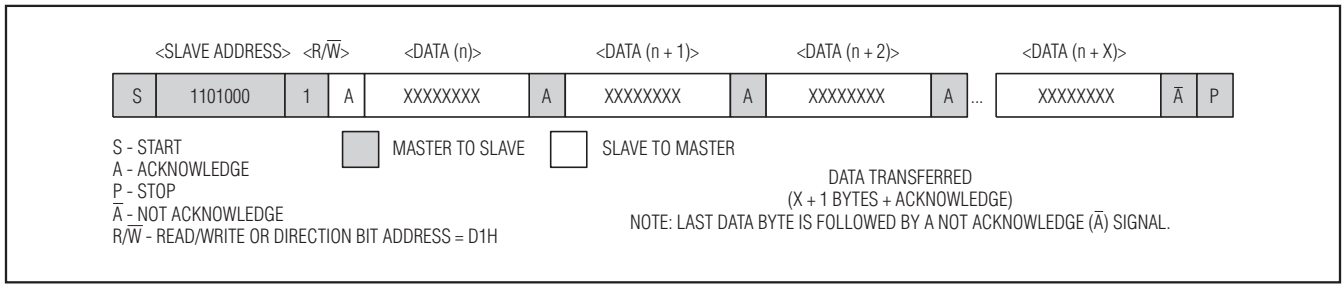

Figure 4. Data Read—RTC Slave Transmitter Mode

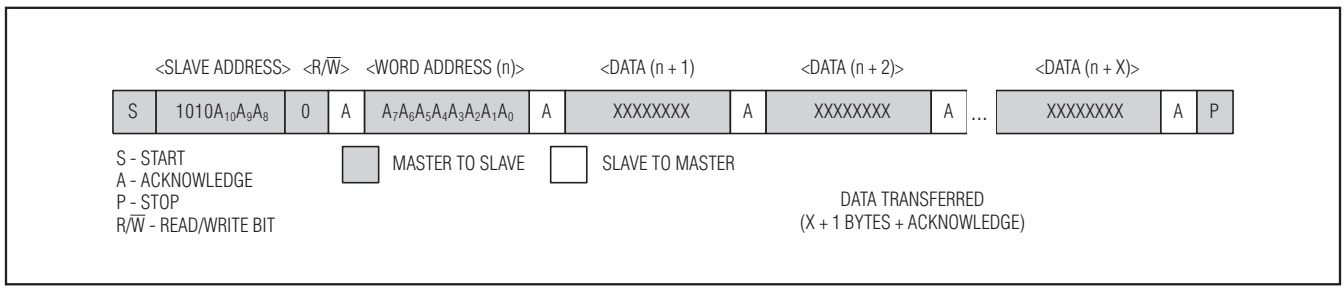

Figure 5. Data Write—DS32B35 FRAM Slave Receiver Mode

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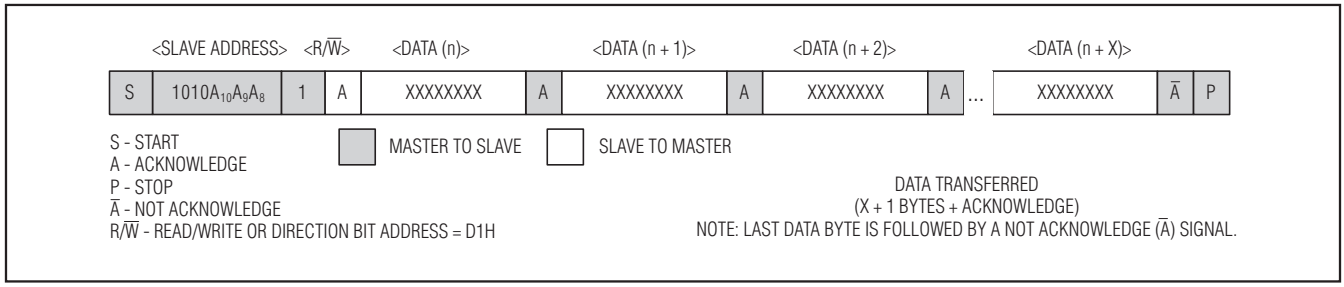


Figure 6. Data Read—DS32B35 FRAM Slave Transmitter Mode

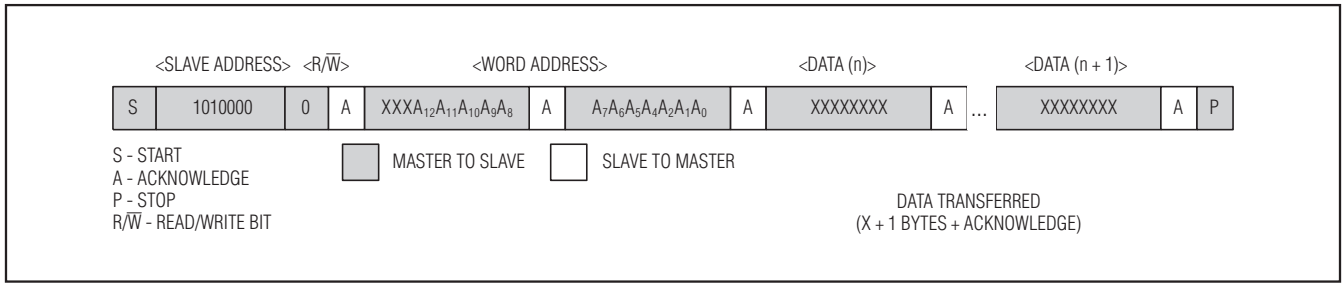


Figure 7. Data Write—DS32C35 FRAM Slave Receiver Mode

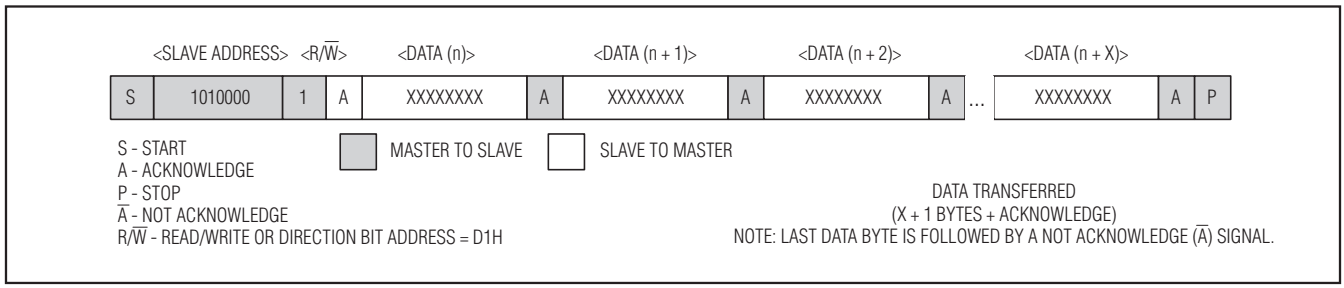


Figure 8. Data Read—DS32C35 FRAM Slave Transmitter Mode

Handling, PCB Layout, and Assembly

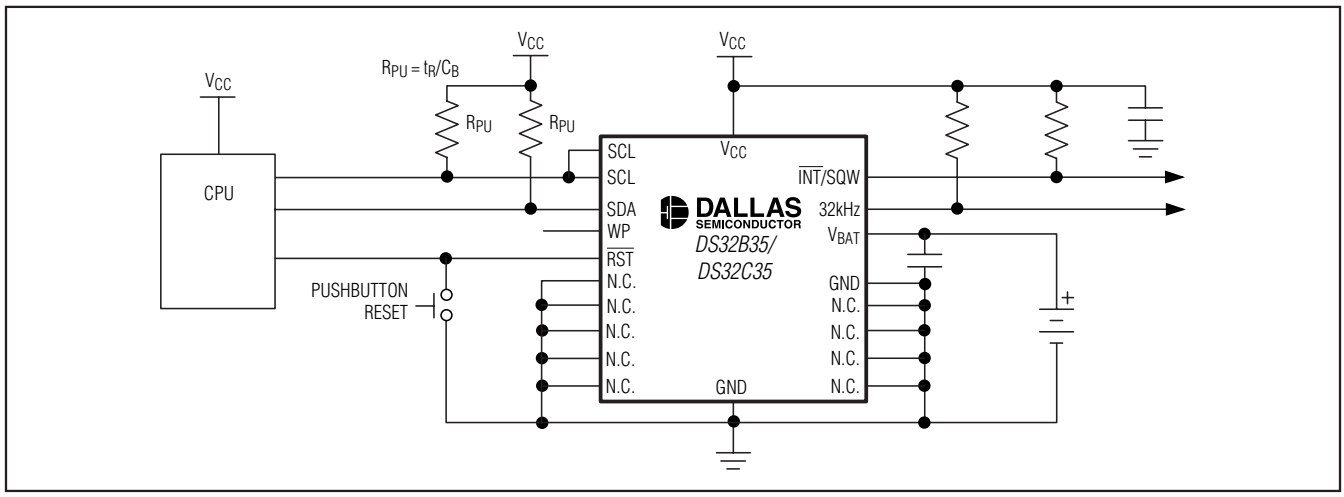
The DS32B35/DS32C35 package contains a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connection) pins must be connected to ground.

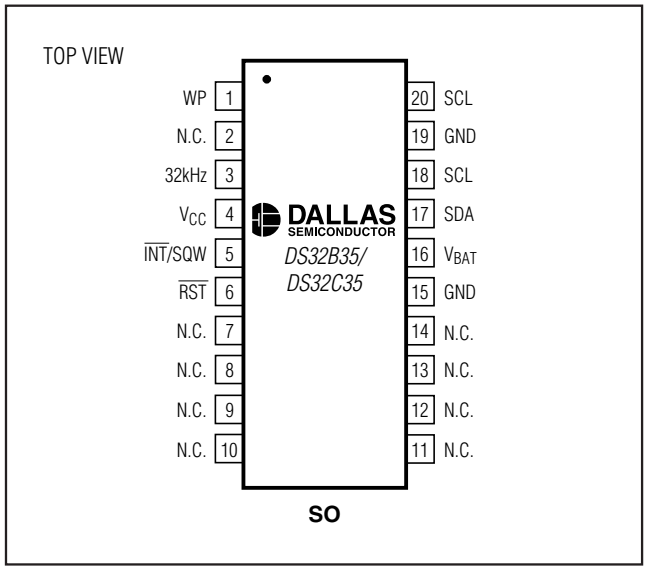
Moisture-sensitive packages are shipped from the factory dry packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications and reflow profiles. Exposure to reflow is limited to 2x maximum.

Accurate I²C RTC with Integrated TCXO/Crystal/FRAM

Typical Operating Circuit



Pin Configuration



Chip Information

SUBSTRATE CONNECTED TO GROUND

PROCESS: CMOS

Selector Guide

PART	FRAM DENSITY	TOP† MARK
DS32B35-33#	2k x 8	DS32B35
DS32B35-33IND#	2k x 8	DS32B35
DS32C35-33#	8k x 8	DS32C35
DS32C35-33IND#	8k x 8	DS32C35

 # Denotes a RoHS-compliant device that may include lead that is exempt under RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes. A "#" anywhere on the top mark denotes a RoHS-compliant device.

†An "N" anywhere on the top mark denotes an industrial grade device.

Thermal Information

Theta-JA: +73°C/W

Theta-JC: +23°C/W

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 SO (300 mils)	—	**56-G4009-001**

Accurate I²C RTC with Integrated TCXO/Crystal/FRAM

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/06	Initial release.	—
1	1/08	Changed data sheet title/references to DS32x35 with DS32B35/DS32C35.	1–21
		Added text to the *General Description* section about the clock/date operation.	1
		In Table 3, changed 04h range from 00–31 to 01–31.	12
2	4/08	Updated the RTC descriptions in the *General Description* and *Detailed Description* sections.	1, 9
		In the Power-Switch Characteristics table, changed t_{REC} max from 2ms to 200ms; added $\overline{RST}$ state information to Note 13.	3
		In the *Typical Operating Characteristics* section, replaced TOCs 1 to 4.	7
		Changed Table 1 column headings; added information about the POR state of the time and date registers to the end of the *Power Control* section.	10
		In the *Handling, PCB Layout, and Assembly* section, added a limit to the number of passes through reflow.	20